Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. and 2. (Cancelled).

3. (Previously Presented): A recording data processing circuit for processing received data sent at a slower data transmission speed than a data processing speed at which to write recording data onto a non-erasable, write-once disk, comprising:

a buffer memory for temporarily storing the received data;

a data processing circuit for preparing the recording data to record onto the disk, based on the received data read from the buffer memory;

a system control circuit for controlling writing and reading of the received data with respect to the buffer memory, and operation of the data processing circuit, and

a writing circuit for writing the recorded data supplied from the data processing circuit, onto the disk,

wherein

the system control circuit suspends operation of the data processing circuit until an amount of received data equivalent to a predetermined writing capacity has been stored in the buffer memory, and releases suspension of the operation of the data processing circuit when an amount of received data equivalent to the predetermined writing capacity has been stored in the buffer memory, said

data processing circuit for recording data being placed in a suspended state by interrupting the power supply or by halting the supply of an operation clock,

wherein

the system control circuit stores an address successive to an address of received data last recorded onto the disk, as a recording start address on the disk, and controls the writing circuit so as to write the recording data supplied from the data processing circuit onto the disk at the recording start address,

and wherein

the system control circuit synchronizes the recording data to be newly recorded onto the disk, supplied from the data processing circuit to the writing circuit, with recording data recorded on the disk, said data processing circuit being operated in synchronism with a reproduction clock obtained by reproducing the data already recorded on the disk.

4. (Original): A recording data processing device according to claim 3, further comprising a motor control circuit for controlling a motor for driving the disk, wherein the motor control circuit controls the motor such that the disk rotates, while operation of the data processing circuit is suspended, at a same speed as that at which the disk rotated immediately before the suspension of data recording.

5. (Original): A recording data processing device according to claim 3, wherein the writing capacity of the buffer memory is set at full memory capacity of the buffer memory.

6. (Original): A recording data processing device according to claim 3, wherein the writing capacity of the buffer memory is set at full memory capacity of

the buffer memory deducted by an amount of data expected to be written into the buffer memory before data recording onto the disk is resumed.

7. and 8. (Cancelled)

9. (Currently Amended): A recording data processing ~~device according to claim 8,~~ circuit for processing received data sent at a slower data transmission speed than a data processing speed at which to write recording data onto a disk, and recording the recording data onto the disk, comprising;

a buffer memory for temporarily storing the received data;

a data processing circuit for preparing the recording data to record onto the disk, based on the received data read from the buffer memory;

a system control circuit for controlling writing and reading of the received data with respect to the buffer memory, and operation of the data processing circuit, and

a writing circuit for writing the recording data supplied from the data processing circuit onto the disk,

wherein

the system control circuit suspends operation of the data processing circuit and writing of the recording data onto the disk by the writing circuit until an amount of received data equivalent to a predetermined writing capacity has been stored in the buffer memory, and releases suspension of the operation of the data processing circuit to resume writing of the recording data onto the disk by the writing circuit when an amount of received data equivalent to the predetermined writing capacity has been stored in the buffer memory, said data processing circuit being placed in a suspended state by interrupting the power supply or by halting the supply of an operation clock;

wherein the system control circuit stores an address successive to an address of received data last recorded onto the disk, as a recording start address on the disk, and controls the writing circuit so as to write the recording data supplied from the data processing circuit onto the disk at the recording start address, and

wherein the system control circuit synchronizes the recording data to be newly recorded onto the disk, supplied from the data processing circuit to the writing circuit, with recording data recorded on the disk, said data processing circuit being operated in synchronism with a reproduction clock obtained by reproducing the data already recorded on the disk.

10. (Original): A recording data processing device according to claim 9, further comprising a motor control circuit for controlling a motor for driving the disk, wherein the motor control circuit controls the motor such that the disk rotates, while operation of the data processing circuit is suspended, at a same speed as that at which the disk rotated immediately before the suspension of data recording.

11. (Original): A recording data processing device according to claim 9, wherein the writing capacity of the buffer memory is set at full memory capacity of the buffer memory.

12. (Original): A recording data processing device according to claim 9, wherein the writing capacity of the buffer memory is set at full memory capacity of the buffer memory deducted by an amount of data expected to be written into the buffer memory before data recording onto the disk is resumed.